UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/436,870	11/09/1999	SHIGERU YOSHINO	450100-02164	7248

20999 7590 12/15/2005

FROMMER LAWRENCE & HAUG
745 FIFTH AVENUE- 10TH FL.
NEW YORK, NY 10151

EXAMINER	
ONUAKU, CHRISTOPHER O	
ART UNIT	**PAPER NUMBER**
2616	

DATE MAILED: 12/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/436,870	YOSHINO ET AL.	
	Examiner	Art Unit	
	Christopher Onuaku	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/26/05*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/26/05 has been entered.

Response to Arguments

2. Applicant's arguments filed 7/6/05 with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Furthermore, applicant argues that Morioka, Pont and Lubbers references are not combinable and that there is a lack of motivation to combine the references.

In response, applicant is reminded that the test for obviousness is not whether the features of the reference may be bodily incorporated into the other to produce the claimed subject matter but simply what the references make obvious to one of ordinary skill in the art. In re Bozek, 163 USPQ 545, (CCPA 1969); In re Richman, 165 USPQ 509, (CCPA 1970); In re Beckum, 169 USPQ 47, (CCPA 1971); In re Sneed, 710 F.2d 1544, 218 USPQ 385. In addition, it is not necessary that the references actually

suggest expressly or in so many words, the changes or improvements that applicant has made. The test for combining references is what the references as a whole would have suggested to one of ordinary skill in the art. In re Sheckler, 168 USPQ 716, (CCPA 1971); In re McLaughlin, 170 USPQ 209, (CCPA 1971); In re Young, 159 USPQ 725, (CCPA 1968).

Applicant's arguments that the combination of Morioka, Pont and Lubbers is improper because it lacks motivation is not persuasive. In each case examiner clearly shows the desirable advantage(s) why Pont should be combined with Morioka and why Lubbers should be combined with Morioka. For example, the desirable advantage of adding the interpolating means of Lubbers to Morioka, which include facilitating the rebuilding or reconstructing of missing data from the external data and the stored calculated parity, is all that would be needed to motivate the artisan to use the Lubbers interpolation means on the Morioka system.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-18&20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morioka et al (US 6,324,334) in view of Pont et al (US 6,014,170) and Lubbers et al (US 5,774,643), and further in view of Bealkowski et al (US 5,826,075).

Regarding claim 1, Morioka et al discloses an apparatus for recording and reproducing data representing video, data representing sound, and other auxiliary data onto/from a disk medium, a tape medium, or a recording/reproducing apparatus which can effectively perform an editing operation and establish a network connected with an external system, comprising:

a) a recording medium (see Fig.1, and data recording HDD 8) which can be accessed at random and plurality input/output processing means (see Fig.1, SCSI-I/F 7, DVC MOVIE camera 11 including DVC CODEC 10 and DVC/PCI I/F 6 and PCI bus 5) for processing input data including video and/or audio data and outputting and recording them in the recording medium and for processing and outputting data reproduced from the reproducing medium (see col.6, line 63 to col.7, line 60);

b) interface means for receiving bit map data externally supplied from a network or memory card separate from the recording medium on which the input data is recorded (see Fig.1, SCSI-I/F 7 and DVC/PCI I/F 6; SVGA-I/F 9; auxiliary/text data which is mixed-in with the video and sound signals to make up the hybrid data signal; col.7, lines 41 to col.8, line 44), here examiner reads bitmap as text data.

Morioka et al fail to explicitly disclose whereby the data recorder-reproducer includes an integral mixer operable to superimpose the bit-map data on data to be recorded by the recorder-reproducer such that the data to be recorded is recorded with the superimposed data, and/or to superimpose the bit-map data on data that is reproduced by the recorder-reproducer.

Pont et al teach an information processing apparatus that connectable to other electronics units so as to form a system to apply specified processing to main image data, sub-image data, and audio data input from the electronic units, and an information processing method therefor, wherein a personal computer (PC) 1 of Fig.1&2, which functions as the information processing apparatus, is connected to a plurality of peripheral units (electronic units), including an electronic camera 5 of Fig.1&3.

Here examiner reads the PC as a recording/reproducing means, because a PC is well known to record data and reproduce data.

Pont et al further teach wherein a bit-map is text data such as characters which is stored in the VRAM 23 of the PC of Fig.2 (see col.3, lines 45-49), and wherein a sub-image data includes a memo written for the main image so as to form a mutual relationship among data (see col.4, lines 1-6 and col.4, lines 37-45). It can be seen from the discussions above that the bit-map data and sub-image data are text data.

Pont teaches, in one embodiment, a procedure executed in the personal computer, wherein the personal computer sends specified commands to the electronic camera 5 to request a transfer of main image data and sub-image data, respectively. And, wherein when the personal computer 1 receives the sub-image data sent from the electronic camera 5, PC 1 applies expansion processing, superimposes the processed sub-image data obtained in expansion processing on the main image data, and writes the main data superimposed with bit-map into the specified area of the VRAM 23 (see col.9, lines 23-29).

Pont fail to explicitly disclose a mixer, but a mixing means is inherent in the Pont et al system in order to efficiently perform the mixing of the main image data with the sub-image data by superimposing the sub-image data on the main image data.

It, therefore, would have been obvious to modify Morioka by realizing Morioka with a mixing means to perform the function of superimposing text data (bit-map/sub-image data) on a main data, for example, wherein the main data with the text data is recorded in a recording medium, as taught by Pont et al.

Furthermore, Morioka and Pont fail to explicitly disclose whereby the data recorder-reproducer includes interpolation means for restoring lost input data by using stored parity data and remaining input data.

Lubbers et al teach Redundant Arrays of Independent Disks (RAID) architecture and systems, including methods and apparatus for enhancing RAID write hole protection and recovery from system failures which would normally leave a "write hole", wherein RAID level 5 uses a technique (1) that writes a block of data across disks (i.e., striping), (2) calculates an error correction code (ECC, i.e., parity) at the bit level from this data and stores the code on another disk, and (3) in the event of a single disk failure, uses the data on the working drives and the calculated code to "Interpolate" what the missing data should be (i.e., rebuilds or reconstructs the missing data from the existing data and the calculated parity) (see col.3, lines 14-27).

It would have been obvious to further modify Morioka by realizing Morioka with an interpolating means to rebuild or reconstruct a missing data from the existing data and the stored calculated parity, as taught by Lubbers et al.

Furthermore, Morioka, Pont and Lubbers fail to explicitly disclose wherein the data recorder-reproducer can perform update of firmware stored in controllers without exchanging ROMs.

Bealkowski et al teach personal computer systems, including an arrangement for storing system firmware, wherein firmware in one memory includes code for checking the validity of firmware stored in another memory and for selecting one or the other of the memories dependent upon a version code of the firmware, and wherein the control means includes an update code for updating the firmware in a selected memory (see Abstract), comprising firmware subsystem 242 and POST (Power-On Self Test) program, which is a set of instructions which execute when the system is first powered on. The system execution of POST is critical to the initialization of the personal computer system 100. Without POST, the system would be unable to load an operating system or other programs (e.g., an update utility program) (see Fig.5A; col.9, line 40 to col.10, line 11). Fig.7&8 show the operation of the update procedure of the firmware subsystem 242 (see col.17, line 45 to col.20, line 30; especially col.19, line 32 to col.20, line 30).

It is noted that in Bealkowski, firmware update is executed without necessarily exchanging ROMs. The process of exchanging ROMs, when firmware updating is required, sometimes results in damaged hardware, and consumes time (see col.20, lines 39-56).

It would have been obvious to further modify Morioka by realizing Morioka with the means to update firmware without necessarily exchanging ROMs, as taught by

Bealkowski, since this provides the desirable advantage of saving time and preventing hardware damage during the process of firmware update. .

Regarding claim 2, Morioka discloses wherein the bit map is input to the interface means through an Ether-network (see col.18, lines 1-7).

Regarding claim 3, Morioka discloses wherein the bit map data is recorded in a detachable memory card and the bit map data recorded in the memory card is received by inserting the memory card into the interface means (see cassette of the Digital Video cassette of the DVC camera 11 which is detachable memory means; col.7, lines 1-60).

Regarding claim 4, Morioka et al discloses an apparatus for recording and reproducing data representing video, data representing sound, and other auxiliary data onto/from a disk medium, a tape medium, or a recording/reproducing apparatus which can effectively perform an editing operation and establish a network connected with an external system, comprising:

a) a recording medium (see Fig.1, and data recording HDD 8) which can be accessed at random and plurality input/output processing means (see Fig.1, SCSI-I/F 7, DVC MOVIE camera 11 including DVC CODEC 10 and DVC/PCI I/F 6 and PCI bus 5) for processing input data including video and/or audio data and outputting and recording them in the recording medium and for processing and outputting data reproduced from the reproducing medium (see col.6, line 63 to col.7, line 6).

b) a rewritable storage means for storing a first control program which is used for processing by at least one of the plural input/output processing means (see Fig.1&4; col.7, line 61 to col.8, line 5; col.10, lines 12-57 and also col.15, lines 40-50), here HDD 8 is the rewritable storage means, and the data processed by the system is stored in the HDD 8 including the control data, or displayed on the NTSC monitor 12 or SVGA monitor 13;

c) interface means for receiving an externally supplied second control program which is used for processing by the at least one of the plural input/output processing means (see Fig.4, keyboard 18, wherein the reproducing speed can be dynamically controlled (changed) in real time by utilizing the keyboard 18; col.10, lines 53-57);

d) rewriting means for rewriting the first control program stored in the storage means into the second control program received by the interface means (see Fig.4, HDD 8 and keyboard 18; col.10, lines 53-57), here when the reproduction speed is changed, the new reproduction speed (second control program) replaces the former reproduction speed (first control program);

e) whereby the data recorder-reproducer includes interpolation means for restoring lost input data by using stored parity data and remaining input data and an integral mixer operable to superimpose the bit-map data on data to be recorded by the recorder-reproducer such that the data to be recorded is recorded with the superimposed data, and/or to superimpose the bit-map data on data that is reproduced by the recorder-reproducer; and wherein the data recorder-reproducer can perform

update of firmware stored in controllers without exchanging ROMs (see claim 1 discussions).

Regarding claim 5, Morioka discloses wherein the first control program data is input to the interface means through an Ethernet-network (see col 18, lines 1-7).

Regarding claim 6, Morioka discloses wherein the second control program data is recorded in a detachable memory card separate from the recording medium on which the input data is recorded and the second control program data recorded in the memory card is received by inserting the memory card into the interface means (see the cassette of the DVC camera 11 which is detachable memory means; col.10, lines 12-57), here the fundamental system configuration in Fig.4 example is the same as that of the Fig.1 example..

Regarding claim 7, Morioka et al discloses an apparatus for recording and reproducing data representing video, data representing sound, and other auxiliary data onto/from a disk medium, a tape medium, or a recording/reproducing apparatus which can effectively perform an editing operation and establish a network connected with an external system, comprising:

a) a recording medium (see Fig.1, and data recording HDD 8) which can be accessed at random at allotted time slots and plurality input/output processing means (see Fig.1, SCSI-I/F 7, DVC MOVIE camera 11 including DVC CODEC 10 and

DVC/PCI I/F 6 and PCI bus 5) for processing input data including video and/or audio data and outputting and recording them in the recording medium and for processing and outputting data reproduced from the reproducing medium (see col.6, line 63 to col.7, line 6);

b) interface means for receiving externally supplied setting data which is used to set at least one of the plural input/out processing means (see Fig.4; I/F 19 and DVC/PCI I/F 6; auxiliary/text data which is mixed-in with the video and sound signals to make up the hybrid data signal; col.10, lines 12-57), here the reproduction speed can be set and reset utilizing the keyboard 18, and the resetting data reads as bit map data, since when the speed is controlled, the application software is applied;

c) setting changing means for changing settings corresponding to the at least one input/output processing means based on the setting data received by the interface means (see Fig.4, keyboard 18; col.10, lines 53-57);

d) whereby the data recorder-reproducer includes interpolation means for restoring lost input data by using stored parity data and remaining input data and an integral mixer operable to superimpose the bit-map data on data to be recorded by the recorder-reproducer such that the data to be recorded is recorded with the superimposed data, and/or to superimpose the bit-map data on data that is reproduced by the recorder-reproducer; and wherein the data recorder-reproducer can perform update of firmware stored in controllers without exchanging ROMs (see claim 1 discussions).

Regarding claim 8, the claimed limitations of claim 8 are accommodated in the discussions of claim 5 above.

Regarding claim 9, Morioka discloses wherein the setting data is recorded in a detachable memory card separate from the recording medium on which the input data is recorded and the setting data recorded in the memory card is received by inserting the memory card into the interface means (see cassette of the Digital Video cassette of the DVC camera 11 which is detachable memory means; col.7, lines 1-60).

Regarding claim 10, the claimed limitations of claim 10 are accommodated in the discussions of claim 1 above.

Regarding claim 11, the claimed limitations of claim 11 are accommodated in the discussions of claim 5 above.

Regarding claim 12, the claimed limitations of claim 12 are accommodated in the discussions of claim 3 above.

Regarding claim 13, the claimed limitations of claim 13 are accommodated in the discussions of claim 4 above.

Regarding claim 14, the claimed limitations of claim 14 are accommodated in the discussions of claim 5 above.

Regarding claim 15, the claimed limitations of claim 15 are accommodated in the discussions of claim 6 above.

Regarding claim 16, the claimed limitations of claim 16 are accommodated in the discussions of claim 7 above.

Regarding claim 17, the claimed limitations of claim 17 are accommodated in the discussions of claim 5 above.

Regarding claim 18, the claimed limitations of claim 18 are accommodated in the discussions of claim 9 above.

Regarding claim 20, Morioka discloses wherein the setting data is used to set a first one of the input/output processing means to a second one of the input/out processing means, as discussed in claim 4 above.

5. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Morioka et al in view of Pont et al, Lubbers et al, and Rossi and further on view of Bertram (US 6,011,546).

Regarding claim 19, Morioka et al, Pont et al, Lubbers et al and Rossi fail to explicitly disclose wherein the rewritable storage means is a rewritable flash ROM. Bertram teaches a programming structure for user interfaces, and programs stored in memory devices associated with microcontrollers controlling a display to a user which are constructed in a language which uses layered statements, and a unique connecting character. Bertram further teaches that control programs will be stored in the system RAM or a flash ROM (see col.37, lines 7-22). It would have been obvious to further modify Morioka by adding a flash ROM to Morioka in order to have an alternative storage means for storing control programs, for example.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher Onuaku whose telephone number is 571-272-7379. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, James Groody can be reached on 571-272-7950. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

COO
12/8/05

James J. Groody
Supervisory Patent Examiner
Art Unit 262~~9~~ 2616